UART Controller v1.1

UART Controller IP Core provides a simple asynchronous serial interface for data transmission and reception. UART signalling is implemented at the serial interface. The core provides a parallel data interface and control interface to control the data flow. It performs parallel-to-serial conversion of data received at parallel data interface, and serial-to-parallel conversion of data received at serial interface.

Features

- Full duplex communication, 8-bit data.
- Simple valid-ready handshaking at the data interface of UART transmitter and receiver for ease of integration with FIFOs.
- Configurable parity: Odd, Even, or no parity.
- Built-in Baud Generator with configurable baud rate.
- Built-in CDC synchronizer at the receiver line.

IP Facts

Provided with the IP package	
Design files	SV/V
Test bench	SV/V
On-board test suite (for FPGA testing)	SV/V
License	Open-source with no restrictions
Resources	UART Controller v1.1 - User Guide
FPGA Proven IP	
Tested on	Artix-7 on Basys-3 Board (XC7A-35T-CPG236-1)
Synthesiser	Vivado 2015.4
Resource utilization	129 LUTs, 98 Registers
Core clock	100 MHz
Baud rates	300-115200 bps
Support	
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IP Solutions	Chipmunk Logic™ IP Cores