UART Controller v1.2

UART Controller IP Core provides a simple asynchronous serial interface for data transmission and reception. UART signalling is implemented at the serial interface. The core provides a parallel data interface and control interface to control the data flow. It performs parallel-to-serial conversion of data received at parallel data interface, and serial-to-parallel conversion of data received at serial interface.

Features

- Full duplex communication, 8-bit data.
- Fully independent control over TX and RX. Supports operation in half-duplex mode.
- Configurable parity: Odd, Even, or no parity.
- Configurable no. of stop bits: 1 or 2.
- Built-in Baud Generator with 16-bit pre-scaler and configurable baud rate.
- Break frame transmission/reception.
- 8x oversampling at RX for balanced speed and error tolerance.
- Error detection: Frame and Parity errors.
- Internal loopback support for testing.
- Simple valid-ready handshaking at the data interface of UART transmitter and receiver for ease of integration with FIFOs.

IP Facts

Provided with the IP package	
Design files	SV/V
Test bench	SV/V
On-board test suite (for FPGA testing)	SV/V
License	Open-source with no restrictions
Resources	UART Controller v1.2 - User Guide
FPGA Proven IP	
Tested on	Xilinx Zybo Z7-20 (XC7-Z020-CLG400-1), Artix-7 FPGA based board
Synthesiser	Vivado 2019.2
Resource utilization	142 LUTs, 115 Registers @Targeted core clock = 100 MHz
Core clock	10-100 MHz
Baud rates	300-115200 bps
Support	
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IP Solutions	Chipmunk Logic™ IP Cores