VGA Controller v1.2

IP Documentation

November 2021

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1. VGA Controller

VGA Controller is a soft IP to generate video timing signals to facilitate driving VGA/DVI Monitors. The IP is dynamically configurable for real-time video timing generation.

2. Features

- ✓ Supports clocked progressive videos.
- ✓ Compile-time configurable maximum resolution.
- ✓ Run-time configurable video resolution; active, blanking, sync, and polarity information.
- ✓ Supports standard as well as custom video resolutions.
- ✓ Supports synchronizing the core operation with external frame sync pulse.
- ✓ Timing complied with VESA monitor standard.

3. Overview

Fig 3.1 shows the top-level block diagram of VGA Controller.

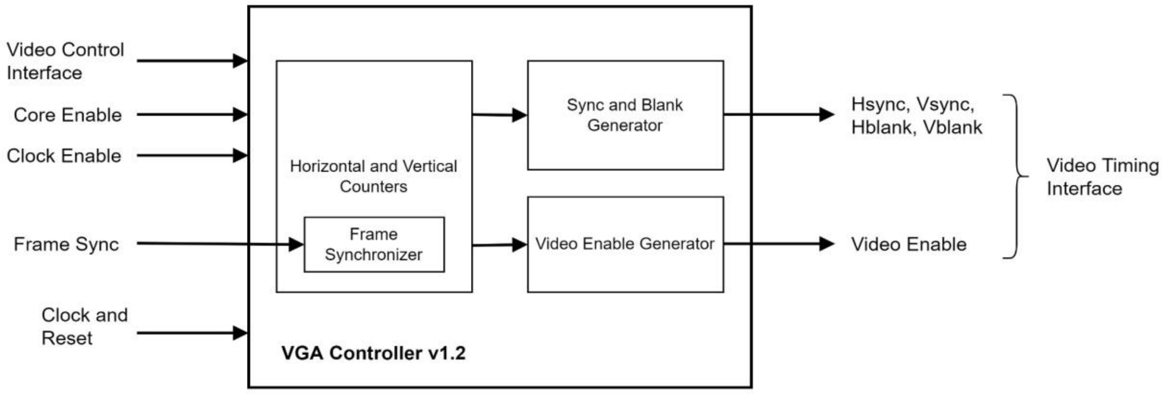

Fig 3.1: VGA Controller – Block Diagram

The core has two primary interfaces: *Video Control* and *Video Timing*.

Video Control Interface is for user to control/configure the core at run-time. It consists of active, blanking, sync, and polarity configuration signals. These signals can be tied to constant, to use the core as a static IP fixed for a specific video resolution.

Video Timing Interface generates all video timing signals as derived from the user configuration.

4. Video Timing

The core can support all standard resolutions as well as custom resolutions configured by user at run-time. Once the core is configured and enabled, video timing signals are generated automatically. The core doesn't require any user intervention thereafter; unless the user wants to change the video resolution.

All timing signals generated are in compliance with VESA monitor standard. Fig 4.1 shows sample video timing for active-high Hsync and Vsync signals.

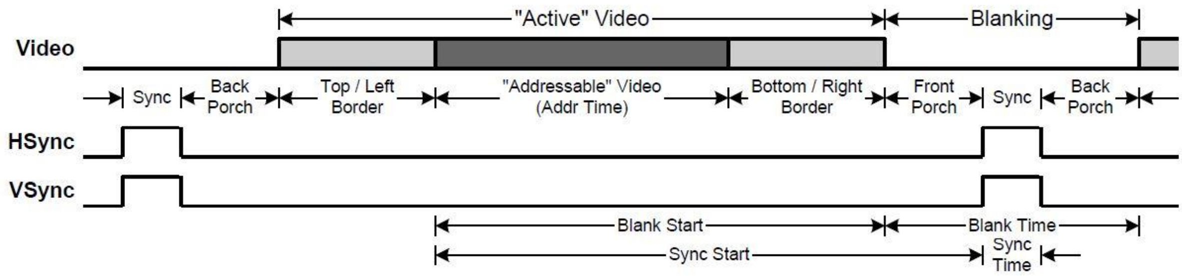

Fig 4.1: Video Timing

5. Configuration Parameters

The core supports compile-time configuration of maximum video resolution supported. Higher the value, more the resource utilization. The resource utilization can thus be controlled/limited as per the requirements of the user using this parameter. Table 4.1 lists all configuration parameters available to the user.

Parameter	Type	Default	Description
`MAX_FWIDTH`	integer	**1920**	Maximum frame width, including blanking. Min. value = 16
`MAX_FHEIGHT`	integer	**1080**	Maximum frame height, including blanking. Min. value = 16

Table 5.1: Configuration Parameters

6. Top-level Ports/Interfaces

Table 5.1 lists all top-level I/O ports/interfaces of VGA Controller.

Signal Name	Direction	Width	Description
clk	input	1	Core Clock
rst	input	1	Core Reset; synchronous, active-high
i_clk_en	input	1	Clock Enable. Refer here for more details.
i_core_en	input	1	Core Enable; enables the IP to generate video timing.
i_fsync	input	1	Frame Sync pulse to synchronize the generation of video timing. Refer here for more details.
Video Control Interface			
i_hsync_pol	input	1	Horizontal Sync polarity
i_vsync_pol	input	1	Vertical Sync polarity
i_hdisp	input	ceil($\log_2$(MAX_FWIDTH))	Active Video width
i_hfront	input	ceil($\log_2$(MAX_FWIDTH))	Horizontal Front Porch
i_hsync_len	input	ceil($\log_2$(MAX_FWIDTH))	Horizontal Sync pulse width
i_hback	input	ceil($\log_2$(MAX_FWIDTH))	Horizontal Back Porch
i_vdisp	input	ceil($\log_2$(MAX_FHEIGHT))	Active Video height
i_vfront	input	ceil($\log_2$(MAX_FHEIGHT))	Vertical Front Porch
i_vsync_len	input	ceil($\log_2$(MAX_FHEIGHT))	Vertical Sync pulse width
i_vback	input	ceil($\log_2$(MAX_FHEIGHT))	Vertical Back Porch
Video Timing Interface			
o_data_en	output	1	Video Enable
o_hblank	output	1	Horizontal Blank
o_hsync	output	1	Horizontal Sync
o_vblank	output	1	Vertical Blank
o_vsync	output	1	Vertical Sync

Table 6.1: Top-level I/O Ports/Interfaces

7. Designing with the IP

This chapter discusses the guidelines, performance, and other known limitations while designing with VGA Controller.

7.1 Clocking

The core has a single clock. The clock should be faster or equal to the pixel rate required. Refer to VESA monitor standard for pixel rates required for different resolutions and refresh rates.

7.2 Reset

The external reset should be synchronous to clock. Single cycle pulse is enough to reset the core.

7.3 Configuring the IP

The IP is configurable at run-time via *Video Control Interface*. The core provides frame-by-frame control. All control signals at *Video Control Interface* are buffered to ensure that no intra-frame artifacts/mistiming occur if the configuration is modified by user while a frame is being rendered by the core. Recommended sequencing for configuring the IP is:

1. Reset the IP.
2. Configure all necessary control signals at *Video Control Interface*.
3. Set Core Enable to 'high'.
4. If required, pulse `i_fsync` to start generating timing in synchronization with this pulse.

7.4 Frame Synchronization

The core's operation can be synchronized with external frame sync pulse at `i_fsync` at any point of time. On asserting this signal, the core resets all its counters. The core starts re-generating video timing once `i_fsync` is de-asserted.

The core re-generates timing based on the current configuration. IP configuration is buffered every frame; hence the timing for new configuration may be generated only after a frame latency in the worst case.

If low-latency operation is required after the IP configuration, `i_fsync` can be pulsed at the beginning. The signal `i_fsync` need to be pulsed only for one clock cycle. If this signal is unused, it should be tied to 'low'.

7.5 Clock Enable to control pixel rate

Clock Enable signal can be used to control pixel rate. This signal has to be asserted for normal operation. De-asserting this signal will stall the core's operation. Clock Enable can be used to control pixel rate in case Core Clock is faster than pixel rate required.

If Core Clock is faster than pixel rate, Clock Enable can be pulsed at appropriate intervals to generate video timing at pixel rate. Clock Enable is then oversampled by Core Clock to generate video timing. This is equivalent to clocking the core at pixel rate. However, user should take into consideration how accurate the derived pixel rate is after oversampling.

If Core Clock is same as pixel rate, then Clock Enable can be simply tied to 'high'.

8. Appendix

8.1 Example Design and Testing

The IP comes with two synthesisable example designs to test a VGA Controller based video system on board. There are two example designs provided for testing:

- Module ***video_top_clken*** to test VGA Controller with Clock Enable to control pixel rate. This is portable RTL across all platforms to test any video resolution as configured by user. Simple color pattern is tested. By default, 640 x 480p is tested.
- Module ***video_top_pll*** to test VGA Controller with PLL to generate pixel clock from an external system clock. This is compatible with designs that instantiate PLL, and can be configured to any video resolution. Simple color pattern in background with moving text is tested. By default, 1280 x 720p HD is tested.

The test framework is shown in Fig 8.1. The 12-bit RGB digital output can be interfaced to any VGA/DVI compatible display through a Video DAC like ADV7125 / Simple Resistor-network DAC / RGB Encoder IC to view the video.

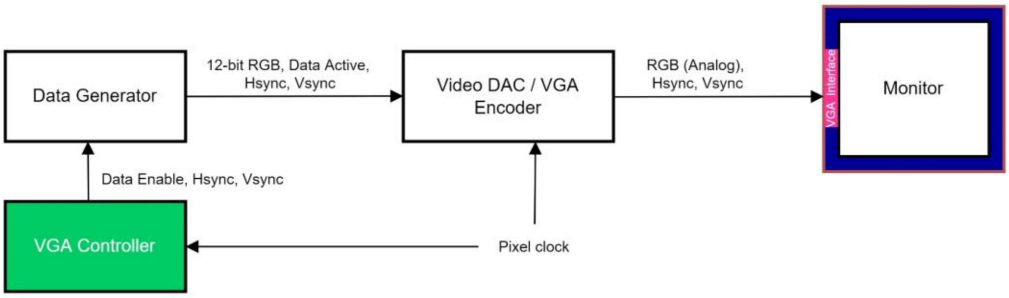

Fig 8.1: VGA Controller On-board Testing

8.2 Performance and Resource Utilization on FPGA

The following is an estimate of timing and resource utilization of ***VGA Controller v1.2*** configured to support up to 1920 x 1080p Full HD when targeted on Xilinx Artix-7 FPGA.

IP Configuration	`MAX_FWIDTH = 2048` `MAX_FHEIGHT = 2048`
FPGA Targeted	Xilinx Basys-3 Board (XC7A-35T-CPG236-1)
Synthesiser	Vivado 2018.3
Targeted Clock Frequency	148.5 MHz, timing verified up to 200 MHz.
LUTs	133
Registers	131

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An open-source licensed IP core

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