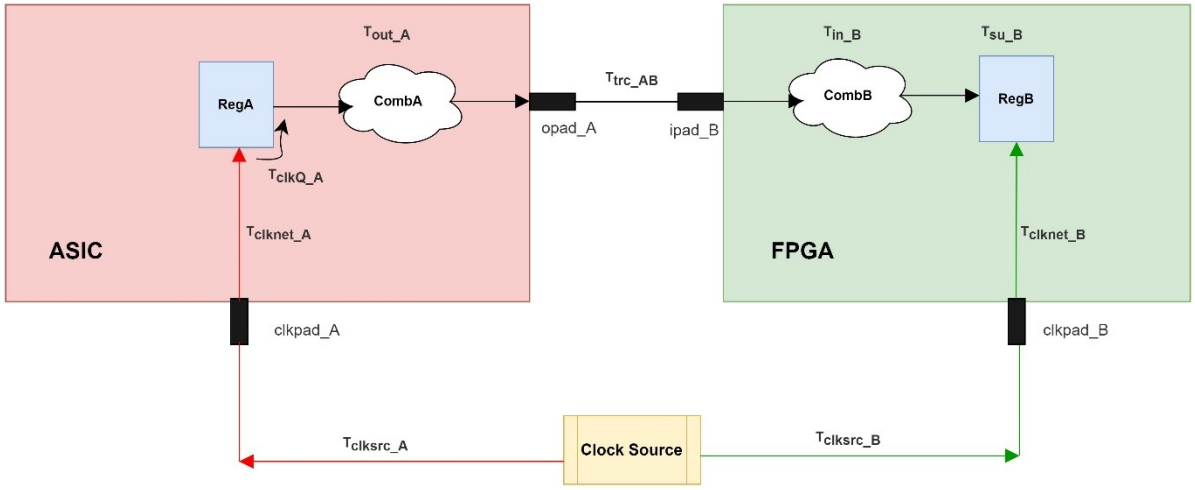
# Constraining Input delay or IO-to-Reg delay at FPGA

In this section, we see how to constraint IO-to-Reg path in FPGA for STA. Assume that an external chip, ASIC is sending data to FPGA. Both ASIC and FPGA are in the same clock domain, launching and sampling data at rising edges.




| S. No | Parameter | Description |
|---|---|---|
| 1 | $T_{clk}$ | Period of clock driving $RegA$ and $RegB$ |
| 2 | $T_{clksrc_A}$ | Source latency of clock from Clock source to $clkpad_A$ |
| 3 | $T_{clknet_A}$ | Network latency of clock from $clkpad_A$ to $RegA$ |
| 4 | $T_{clkQ_A}$ | Clock-to-Q delay of $RegA$ |
| 5 | $T_{out_A}$ | Combinatorial + route delay from $RegA$ to $opad_A$ |
| 6 | $T_{clksrc_B}$ | Source latency of clock from Clock source to $clkpad_B$ |
| 7 | $T_{clknet_B}$ | Network latency of clock from $clkpad_B$ to $RegB$ |
| 8 | $T_{trc_AB}$ | Trace delay between $opad_A$ and $ipad_B$ |
| 9 | $T_{in_B}$ | Combinatorial + route delay from $ipad_B$ to $RegB$ |
| 10 | $T_{su_B}$ | Setup time of $RegB$ |
| 11 | $T_{ho_B}$ | Hold time of $RegB$ |
| 12 | $T_{uncty}$ | Clock uncertainty: jitter, OCV etc |

Clock Source is where the clock originates from, $clkpad_B$ is where clock definition happens at FPGA.

## Setup Analysis

For Setup Analysis, consider **max Data path**, **max Source clock (launching clock) path**, **min Destination clock (sampling clock) path**. And then compute **Data Arrival** and **Data Required Times**.

### Data Arrival and Data Required Times

To satisfy Setup Timing:

$$\boxed{\begin{array}{c} \textit{Data Arrival Time} \le \textit{Data Required Time} \\ \textit{Slack} = \textit{Data Required Time} - \textit{Data Arrival Time} \ge 0 \end{array}}$$

$$\underbrace{(T_{clksrc_A_max} + T_{clknet_A_max})}_{\textit{Source clock path}} + \underbrace{(T_{clkQ_A_max} + T_{out_A_max}) + T_{trc_AB_max} + (T_{in_B_max} + T_{su_B})}_{\textit{Data path}}$$

$$\le \underbrace{T_{clk} + T_{clksrc_B_min} + T_{clknet_B_min} - T_{uncty}}_{\textit{Destination clock path}} \qquad \text{----------} \ (1)$$

- $T_{clknet_A_max} + T_{clkQ_A_max} + T_{out_A_max}$ = max $clkpad_A$ to $opad_A$ delay, which is usually specified in ASIC datasheet as: **max output delay**, $T_{oA_max}$ .
- $T_{in_B_max} + T_{su_B}$ = max $ipad_B$ to $RegB$ delay, $T_{iB_max}$ , which is already known/computed by STA tool at FPGA side after place and route.

Therefore $(1)$ becomes:

$$T_{clksrc_A_max} + T_{oA_max} + T_{trc_AB_max} + T_{iB_max} \le T_{clk} + T_{clksrc_B_min} + T_{clknet_B_min} - T_{uncty}$$

$$\Rightarrow$$

$$\boxed{T_{clksrc_A_max} + T_{oA_max} + T_{trc_AB_max} - T_{clksrc_B_min} + T_{iB_max} \le T_{clk} + T_{clknet_B_min} - T_{uncty}}$$

Yellow fields signify the unknown parameters to STA tool that make up the **max input delay**, which has to be conveyed to STA tool through `set_input_delay` SDC constraint and virtual clock. This constraint is then used for **Setup / Max Path / Slow Process Corner Analysis**, for e.g.:

```
create_clock -name clk -period 10.000 [get_ports clkpad_B]
create_clock -name vclk -period 10.000
derive_clock_uncertainty
set tclksrc_A_max 0.200
set toA_max 0.500
set ttrc_AB_max 0.200
set tclksrc_B_min 0.100
set tinp_max [expr $tclksrc_A_max + $toA_max + $ttrc_AB_max - tclksrc_B_min]
set_input_delay -clock vclk -max $tinp_max [get_ports ipadB]
```

## Hold Analysis

For Hold Analysis, consider **min Data path**, **min Source clock (launching clock) path**, **max Destination clock (sampling clock) path**. And then compute **Data Arrival** and **Data Required Times**.

### Data Arrival and Data Required Times

To satisfy Hold Timing:

$$\boxed{\begin{array}{c} \textit{Data Arrival Time} \geq \textit{Data Required Time} \\ \textit{Slack} = \textit{Data Arrival Time} - \textit{Data Required Time} \geq 0 \end{array}}$$

$$\underbrace{(T_{clksrc_A_min} + T_{clknet_A_min})}_{\textit{Source clock path}} + \underbrace{(T_{clkQ_A_min} + T_{out_A_min}) + T_{trc_AB_min} + (T_{in_B_min} - T_{ho_B})}_{\textit{Data path}}$$

$$\geq \underbrace{T_{clksrc_B_max} + T_{clknet_B_max} + T_{uncty}}_{\textit{Destination clock path}} \qquad \text{----------} \ (2)$$

- $T_{clknet_A_min} + T_{clkQ_A_min} + T_{out_A_min}$ = min $clkpad_A$ to $opad_A$ delay, which is usually specified in ASIC datasheet as: **min output delay**, $T_{oA_min}$. This parameter is often not seen in datasheets, in that case, assume a derated value from **typical output delay**, given in datasheet.
- $T_{in_B_min} - T_{ho_B}$ = min $ipad_B$ to $RegB$ delay, $T_{iB_min}$, which is already known/computed by STA tool at FPGA side after place and route.

Therefore $(2)$ becomes:

$$T_{clksrc_A_min} + T_{oA_min} + T_{trc_AB_min} + T_{iB_min} \geq T_{clksrc_B_max} + T_{clknet_B_max} + T_{uncty}$$

$$\Rightarrow$$

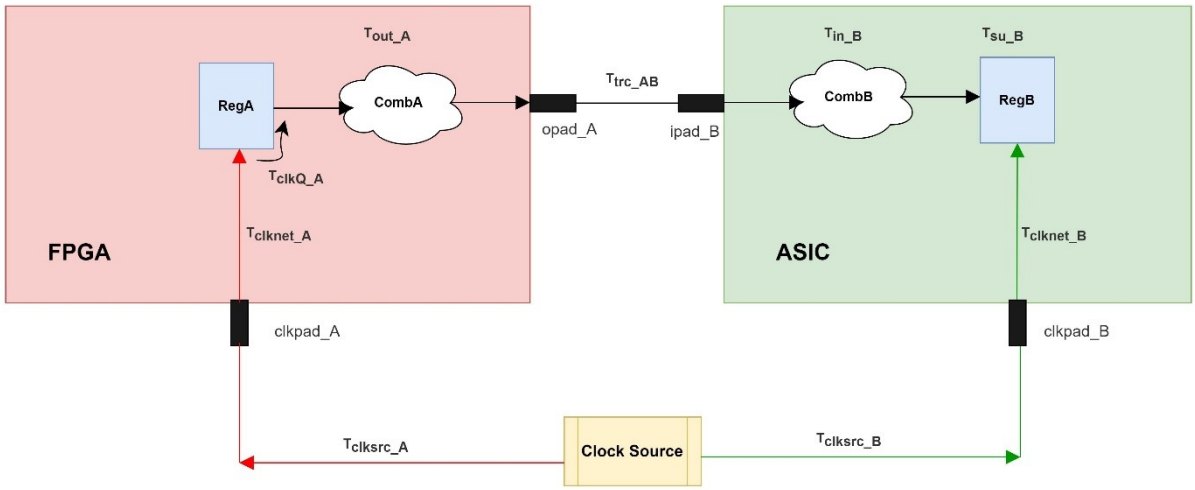
$$\boxed{T_{clksrc_A_min} + T_{oA_min} + T_{trc_AB_min} - T_{clksrc_B_max} + T_{iB_min} \geq T_{clknet_B_max} + T_{uncty}}$$

Yellow fields signify the unknown parameters to STA tool that make up the **min input delay**, which has to be conveyed to STA tool through `set_input_delay` SDC constraint and virtual clock. This constraint is then used for **Hold / Min Path / Fast Process Corner Analysis**, for e.g.:

```
create_clock -name clk -period 10.000 [get_ports clk]
create_clock -name vclk -period 10.000
derive_clock_uncertainty
set tclksrc_A_min 0.150
set toA_min 0.400
set ttrc_AB_min 0.100
set tclksrc_B_max 0.200
set tinp_min [expr $tclksrc_A_min + $toA_min + $ttrc_AB_min - tclksrc_B_max]
set_input_delay -clock vclk -min $tinp_min [get_ports ipadB]
```

## Constraining Output delay or Reg-to-IO delay at FPGA

In this section, we see how to constraint Reg-to-IO path in FPGA for STA. Assume that FPGA sending data to an external chip, ASIC. Both FPGA and ASIC are in the same clock domain, launching and sampling data at rising edges.




| S. No | Parameter | Description |
|---|---|---|
| 1 | $T_{clk}$ | Period of clock driving $RegA$ and $RegB$ |
| 2 | $T_{clksrc_A}$ | Source latency of clock from Clock source to $clkpad_A$ |
| 3 | $T_{clknet_A}$ | Network latency of clock from $clkpad_A$ to $RegA$ |
| 4 | $T_{clkQ_A}$ | Clock-to-Q delay of $RegA$ |
| 5 | $T_{out_A}$ | Combinatorial + route delay from $RegA$ to $opad_A$ |
| 6 | $T_{clksrc_B}$ | Source latency of clock from Clock source to $clkpad_B$ |
| 7 | $T_{clknet_B}$ | Network latency of clock from $clkpad_B$ to $RegB$ |
| 8 | $T_{trc_AB}$ | Trace delay between $opad_A$ and $ipad_B$ |
| 9 | $T_{in_B}$ | Combinatorial + route delay from $ipad_B$ to $RegB$ |
| 10 | $T_{su_B}$ | Setup time of $RegB$ |
| 11 | $T_{ho_B}$ | Hold time of $RegB$ |
| 12 | $T_{uncty}$ | Clock uncertainty: jitter, OCV etc |

Clock Source is where the clock originates from, $clkpad_A$ is where clock definition happens at FPGA.

## Setup Analysis

For Setup Analysis, consider **max Data path**, **max Source clock (launching clock) path**, **min Destination clock (sampling clock) path**. And then compute **Data Arrival** and **Data Required Times**.

### Data Arrival and Data Required Times

To satisfy Setup Timing:

$$\boxed{\begin{array}{c} \textit{Data Arrival Time} \le \textit{Data Required Time} \\ \textit{Slack} = \textit{Data Required Time} - \textit{Data Arrival Time} \ge 0 \end{array}}$$

$$\underbrace{(T_{clksrc_A_max} + T_{clknet_A_max})}_{\textit{Source clock path}} + \underbrace{(T_{clkQ_A_max} + T_{out_A_max}) + T_{trc_AB_max} + (T_{in_B_max} + T_{su_B})}_{\textit{Data path}}$$

$$\le \underbrace{T_{clk} + T_{clksrc_B_min} + T_{clknet_B_min} - T_{uncty}}_{\textit{Destination clock path}} \qquad \text{----------} \ (3)$$

- $T_{clknet_A_max} + T_{clkQ_A_max} + T_{out_A_max}$ = max $clkpad_A$ to $opad_A$ delay, $T_{oA_max}$, which is already known/computed by STA tool at FPGA side after place and route.
- $T_{in_B_max} + T_{su_B} - T_{clknet_B_min}$ = $ipad_B$ to $clkpad_B$ setup time, which is usually specified in ASIC datasheet as: **data setup time**, $T_{isuB_max}$.

Therefore $(3)$ becomes:

$$T_{clksrc_A_max} + T_{clknet_A_max} + T_{clkQ_A_max} + T_{out_A_max} + T_{trc_AB_max} + T_{isuB_max}$$

$$\le T_{clk} + T_{clksrc_B_min} - T_{uncty}$$

$$\Rightarrow$$

$$\boxed{\begin{array}{l} T_{clknet_A_max} + T_{clkQ_A_max} + T_{out_A_max} \\ \le T_{clk} - (T_{clksrc_A_max} + T_{trc_AB_max} + T_{isuB_max} - T_{clksrc_B_min}) - T_{uncty} \end{array}}$$

Yellow fields signify the unknown parameters to STA tool that make up the **max output delay**, which has to be conveyed to STA tool through `set_output_delay` SDC constraint and virtual clock. This constraint is then used for **Setup / Max Path / Slow Process Corner Analysis**, for e.g.:

```
create_clock -name clk -period 10.000 [get_ports clkpad_A]
create_clock -name vclk -period 10.000
derive_clock_uncertainty
set tclksrc_A_max 0.200
set tisuB_max 0.500
set ttrc_AB_max 0.200
set tclksrc_B_min 0.100
set toutp_max [expr $tclksrc_A_max + $tisuB_max + $ttrc_AB_max - tclksrc_B_min]
set_output_delay -clock vclk -max $toutp_max [get_ports opadA]
```

## Hold Analysis

For Hold Analysis, consider **min Data path**, **min Source clock (launching clock) path**, **max Destination clock (sampling clock) path**. And then compute **Data Arrival** and **Data Required Times**.

### Data Arrival and Data Required Times

To satisfy Hold Timing:

$$\boxed{\begin{array}{c} \textit{Data Arrival Time} \geq \textit{Data Required Time} \\ \textit{Slack} = \textit{Data Arrival Time} - \textit{Data Required Time} \geq 0 \end{array}}$$

$$\underbrace{(T_{clksrc_A_min} + T_{clknet_A_min})}_{\textit{Source clock path}} + \underbrace{(T_{clkQ_A_min} + T_{out_A_min}) + T_{trc_AB_min} + (T_{in_B_min} - T_{ho_B})}_{\textit{Data path}}$$

$$\geq \underbrace{T_{clksrc_B_max} + T_{clknet_B_max} + T_{uncty}}_{\textit{Destination clock path}} \qquad \text{----------} \ (4)$$

- $T_{clknet_A_min} + T_{clkQ_A_min} + T_{out_A_min}$ = min $clkpad_A$ to $opad_A$ delay, $T_{oA_min}$, which is already known/computed by STA tool at FPGA side after place and route.
- $T_{ho_B} + T_{clknet_B_max} - T_{in_B_min}$ = $ipad_B$ to $clkpad_B$ hold time, which is usually specified in ASIC datasheet as: **data hold time**, $T_{ihoB_max}$ .

Therefore $(4)$ becomes:

$$T_{clksrc_A_min} + T_{clknet_A_min} + T_{clkQ_A_min} + T_{out_A_min} + T_{trc_AB_min}$$

$$\geq T_{clksrc_B_max} + T_{ihoB_max} + T_{uncty}$$

$$\Rightarrow$$

$$\boxed{\begin{array}{l} T_{clknet_A_min} + T_{clkQ_A_min} + T_{out_A_min} \geq \\ -(T_{clksrc_A_min} + T_{trc_AB_min} - T_{ihoB_max} - T_{clksrc_B_max}) + T_{uncty} \end{array}}$$

Yellow fields signify the unknown parameters to STA tool that make up the **min output delay**, which has to be conveyed to STA tool through `set_output_delay` SDC constraint and virtual clock. This constraint is then used for **Hold / Min Path / Fast Process Corner Analysis**, for e.g.:

```
create_clock -name clk -period 10.000 [get_ports clkpad_A]
create_clock -name vclk -period 10.000
derive_clock_uncertainty
set tclksrc_A_min 0.150
set tihoB_max 0.400
set ttrc_AB_min 0.100
set tclksrc_B_max 0.200
set toutp_min [expr $tclksrc_A_min - $tihoB_max + $ttrc_AB_min - tclksrc_B_max]
set_output_delay -clock vclk -min $toutp_min [get_ports opadA]
```